Materials Science in Semiconductor Processing 37 (2015) 9–13

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Improvement of data retention characteristics of OSOSO multi-stacked MIS capacitor for flat panel display technology

Jayapal Raja [a], Sungwook Jung [a], Kyungsoo Jang [a], Zhenghai Jin [a], Somenath Chatterjee [b], S Velumani [a,c], Jiwoong Kim [a], Junsin Yi [a,*]

[a] College of Information and Communication Engineering, Sungkyunkwan University, Suwon 440-746, Republic of Korea
[b] Department of Electronics and Communication Engineering, Sikkim Manipal Institute of Technology, Sikkim Manipal University, Sikkim 737-136, India
[c] Department of Electrical Engineering (SEES), CINVESTAV-IPN, Col. San Pedro Zacatenco, Mexico City 07360, Mexico

ARTICLE INFO

Available online 19 January 2015

Keywords:
Stacked NVM
Oxide–Silicon–Oxynitride–Silicon–Oxynitride (OSOSO)
System-On-Panel (SOP) display

ABSTRACT

The data retention ability in metal–oxide–silicon–oxynitride–silicon (MOSOS) devices can be improved using a thicker tunneling layer and novel multi-stacked oxide–silicon–oxynitride–silicon–oxynitride (OSOSO) structure. The OSOSO devices showed 7 fold increase (53.5%) of data retention after a decade compared to OSO devices (6.71%). The improvement in data retention is attributed to the excellent resistance of the charge retention due to the redistribution of electric field across the multi-stacked layers. The spilt storage layer provided a room for storing more charges in different positions of the layers resulting in ~2–3 times increase in memory window. Hence, the performances of those devices are suitable for data storage application in the system-on-panel (SOP) display.

1. Introduction

Polycrystalline silicon thin film non-volatile memory (poly-Si NVM) is a key component in flat panel displays (FPDs) of SOP technology. FPDs with built-in NVM devices have attracted much attention in SOP [1–3] to support various multiple applications [4–11], such as; data, image and signal storage owing to their ability of low-power consumption, high-charge storage and long-data retention with low power operation. Many research groups [6–11] have reported the fabrication and characterization of poly-Si thin film NVM devices with an oxide–nitride–oxide (ONO) stacked structure. However, these devices have some limitations regarding the above mentioned applications. As described in our earlier publication, the ultra-thin oxynitrided ONO layer for low temperature poly-Si (LTPS) NVM devices utilize high power [7]. Again, LTPS NVM devices with silicon-oxynitride (SiO_xN_y) tunneling layer using plasma-assisted oxynitridation is not compatible with a uniform and ultra-thin tunneling layer [7,10].

Previously, we studied the advantage of oxide–silicon–oxynitirde (OSO) structure for poly-Si NVM devices [12] that achieve higher storage capacity and low operating voltage compared to ONO stacked devices. However, the fabricated metal–OSO–semiconductor (MOSOS) devices using OSO stack with a 2.7 nm ultra-thin oxynitride layer on Si substrate provided poor retention characteristics (discussed in Section 3). To overcome the above issues, a MOSOS device is considered following two approaches- i) increase the thickness of the tunneling layer and ii) multi-stack structures (i.e. OSOSO). The concept of multi-layers of Si nanocrystals have been employed for better data retention and multilevel charge storage of NVMs [13,14]. In our paper, the tunneling layer thickness is increased from 2.7 nm to 3.9 nm whereas

* Corresponding author. Tel.: +82 31 290 7139.
E-mail address: yi@yurim.skku.ac.kr (J. Yi).

http://dx.doi.org/10.1016/j.mssp.2014.12.037
1369-8001/

the same charge-trapping and blocking layer thickness are considered. In addition, we use a novel OSOSO multi-stacked structure to create a simple and improved metal–insulator–semiconductor (MIS) type device fabrication.

Our OSOSO stack structure in MOSOSOS (metal–OSOSO–semiconductor) device contains an ultra-thin double SiO_xN_y film as the tunneling layer, double a-Si film as the storage layer and single Silicon di-oxide (SiO_2) film as a blocking layer on a Si substrate. An improved data retention and large memory window are shown with the comparison of our proposed thicker tunneling layer of OSOSO multi-stacked structure and previously reported OSO structure.

2. Experimental details

A n-type (100) crystalline Si wafer was used as substrate to fabricate MOSOS and MOSOSOS devices, which was much cleaner and smoother than the low-temperature poly-Si on glass used by Jung group [10]. After standard cleaning, the OSO stack structure was formed with a oxynitride layer of 2.7 nm and 3.9 nm thick using the plasma-assisted oxynitridation method in an inductively coupled plasma-chemical vapor deposition (ICP–CVD) system. A oxynitride layer was deposited on Si wafers by nitrous oxide (N_2O) plasma exposure using a N_2O gas flow rate of 2.5 sccm, radio frequency (RF) power of 150 W, and substrate temperature of 300 °C. By controlling the duration of N2O plasma treatment, the different thicknesses of the thin SiO_xN_y film were deposited. In addition, amorphous Si (a-Si) film with a thickness of 10 nm and a SiO_2 blocking layer with a thickness of 20 nm were deposited by ICP–CVD system. The process condition for a-Si film (charge-trapping layer) were H_2/SiH_4 gas ratio of 30, RF power of 200 W, and temperature of 300 °C, respectively. An a-Si film deposited with above condition has the maximum charge-trapping sites in a-Si thin film and interface between a-Si and SiO_2/SiO_xN_y layers. The detailed process and results can be found elsewhere [12]. An Al electrode for the MOSOS structure was formed by thermal evaporation technique.

The treatment of N_2O plasma and deposition of a-Si thin film were repeatedly accomplished by an ICP–CVD system under the same conditions to fabricate the OSOSO structure. An OSOSO stack structure was initially formed with an ultra-thin tunneling oxynitride layer 2.7 nm thick and a-Si charge-trapping layer with 5 nm thick. The thicknesses of these layers were measured with spectroscopic ellipsometry (VB-250, J.A. Woollam) system with a spectrum response range of 240–1700 nm. The fabricated OSOSO stack structure has two tunneling and charge storage layer. The Al was evaporated as a gate electrode, after the deposition of SiO_2 as a blocking layer. Then, the high frequency (1 MHz) capacitance–voltage (*C–V*) hysteresis and retention characteristics of the fabricated MOSOS and MOSOSOS devices were investigated by using HP 4192A impedance analyzer.

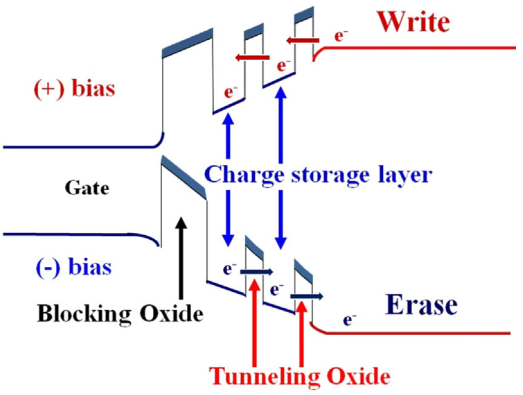

Fig. 1. Principles of OSOSO stack structure under erasing and writing mode.

3. Results and discussion

It is well known that, an a-Si is better charge storage layer than a Si_3N_4 layer for fabrication of NVM devices on glass substrate, because the band gap of a-Si is lower (~1.7 eV) than that of Si_3N_4 (~5 eV). Also, a larger band offsets and existence of the localized trap states in a-Si provides more room for charge storage [12]. Multilayered charge storage NVM memories have been suggested by several researchers [14–16] due to their potential advantage of low charge-loss and a large memory window. Considering the above fact, a multilevel a-Si stacked charge storage layers are used in this study.

Our devices contain a double tunneling barrier of SiO_xN_y and double trap layer of a-Si:H film. These two trapping layers provide greater charge storage in NVM devices. The

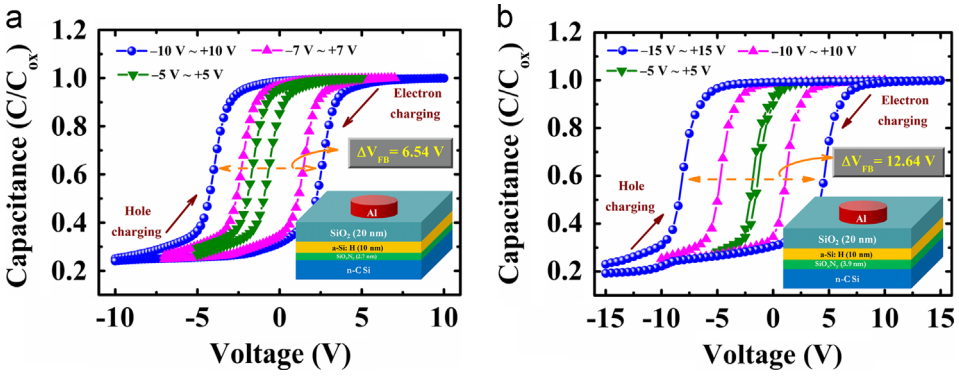

Fig. 2. *C–V* hysteresis curve of fabricated MOSOS devices with OSO stack (a) 20/10/2.7 nm thick and (b) 20/10/3.9 nm thick. The inset is a schematic diagram of the OSO stacked device structure.

principles of the OSOSO multi-stack can be schematically explained by the energy band diagram, shown in Fig. 1. Let us take electrons as carrier for example. When the gate voltage increases, then electrons be able to tunnel [17] into the upper a-Si layer through available levels in the lower a-Si layer. Those electrons would be relaxed to the localized trap centers and stored on the lower and upper trap centers. Reverse process is applicable for discharging process.

Fig. 2 shows the *C–V* hysteresis characteristics of the fabricated MOSOS devices, as a function of two different tunneling thicknesses. The inset shows OSO stacked device structures. These two OSO stack structures consist of the tunneling SiO_xN_y layer of 2.7 nm and 3.9 nm thick with a top blocking 20 nm thick SiO_2 layer and 10 nm thick a-Si storage layer, respectively. The stability and tunneling capability of the ultra-thin SiO_xN_y layers have been described elsewhere [7]. When the tunnel oxide is ultra-thin (2.7 nm), the voltage sweeps from inversion (-10 V) to accumulation ($+10$ V) and back to inversion (-10 V), is increased greatly due to the flat band voltage shift (ΔV_{FB}) of 6.54 V. The electrons can tunnel easily through an ultra-thin tunneling barrier at low electric fields. On the contrary, due to the thicker oxide (3.9 nm), the ΔV_{FB} values are drastically decreased to 5.87 V. When the thickness of tunnel layer is 2.7 nm, direct tunneling (DT) takes place [17,18]. The lowered memory window indicates the voltage drop over the oxide barrier is insufficient to tunnel electrons from the substrate to a blocking layer. Therefore, it will be a need of greater sweep voltage up to ± 15 V.

As, one can observed from the hysteresis curve in Fig. 2(b), the ΔV_{FB} of 12.64 V in voltage sweeps range from -15 V to $+15$ V and back to -15 V, which has the largest memory window. The band diagram and charge storage mechanisms of the OSO stack devices were explained in our previous report [12]. In this device, the swept voltages are higher due to the thicker tunneling layer than in Fig. 2(a). It is reported that both the DT and F–N (Fowler–Nordhiem) tunneling current contribute to the injection process for the thicker tunneling layer of 3.9 nm [18]. When the applied electric field is high, the F–N tunneling current is dominant. The small ΔV_{FB} of 6.54 V in MOSOS device with the 2.7 nm thin tunneling layer device is due to fast discharge of the injected charge at defect sites of a-Si through the ultra-thin tunneling layer. A larger hysteresis width is observed in the 3.9-nm-thick SiO_xN_y (tunneling layer) device than in the 2.7 nm thick SiO_xN_y device. This is due to the exponential decrease in the degree of tunneling through the tunnel oxides as oxide thickness increases. However, the thicker tunneling layer device prevents the data leakage to ensure a good data storage capability.

Fig. 3 represents the *C–V* hysteresis measurements of the fabricated OSOSO multi-stacked devices. Its structure consists of a top blocking 20 nm thick SiO_2 layer, the double 5 nm thick a-Si storage layer, and double ultra-thin tunneling 2.7 nm thick SiO_xN_y layer. In this multi-stack structure, the injected electrons can be stored (i) at the band gap offset region of the upper and lower a-Si layers (ii) at the trap sites in both a-Si layers, (iii) at the interface states in a-Si/SiO_xN_y layers, and (iv) at the SiO_2/a-Si interface traps. Fig. 3 shows the OSOSO multi-stack has larger ΔV_{FB} than OSO stacks. The memory window increases steadily from 2.5 to 14.39 V with increasing applied gate voltage from ± 5 V to ± 15 V. As we can see, a higher programming bias applied at the gate results in a wider corresponding hysteresis by DT tunneling mechanism. Hence the narrow *C–V* curve in Figs. 2(a) and (b) corresponds to the charging of only one layer and the wider one in Fig. 3 to the charging of two layers. The increment of ΔV_{FB} indicates that more charges are stored in the different layers of the devices. The charge storage may be enhanced using OSOSO multi-stack structure in FPD system. The large

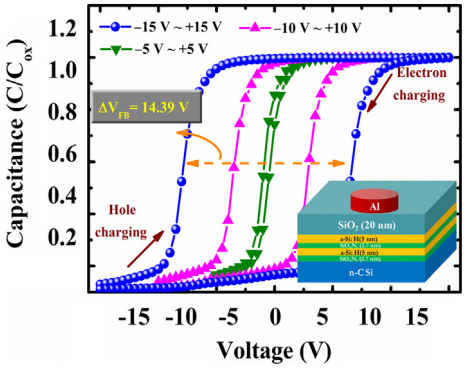

Fig. 3. *C–V* hysteresis curve of fabricated MOSOSOS devices with the OSOSO stack 20/5/2.7/5/2.7 nm thick. The inset is a schematic diagram of the OSOSO stacked device structure.

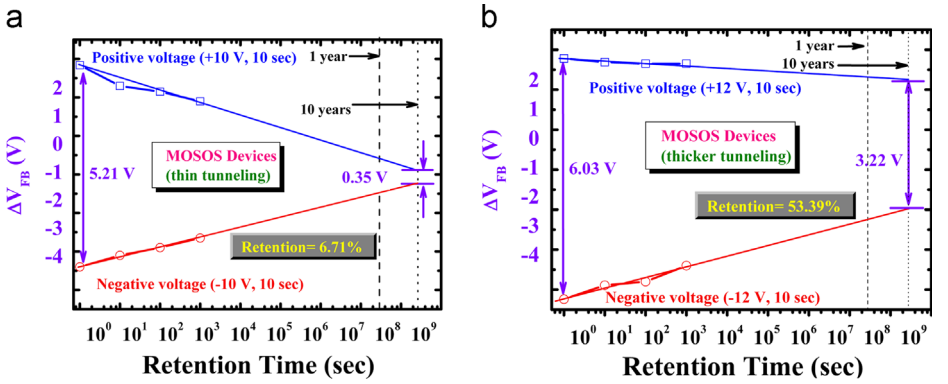

Fig. 4. Charge retention characteristics of fabricated MOSOS devices with an OSO stack of (a) 20/10/2.7 nm thick and (b) 20/10/3.9 nm thick.

memory window reveals the high carrier trapping efficiency for both electrons and holes. These results indicate that the thicker tunneling layer of OSO stack structure or OSOSO multi-stack structure increases the memory window about 2–3 times compared to that of the OSO stack structure.

Study the properties of charge retention of the NVM devices is an important aspect. Fig. 4 illustrates the remaining memory windows after data retention characteristics for MOSOS devices with different tunneling layer thicknesses. The retention characteristics were measured using ΔV_{FB} of the *C–V* curve at bias voltage of $\pm$ 10 V fixing the bias time at 10 s. The ΔV_{FB} between the programming/erasing (P/E) states of the MOSOS device with OSO stack of thicknesses 20/10/2.7 nm was initially 5.21 V and decreased to 0.35 V after 10 years, as shown in Fig. 4(a). The value of ΔV_{FB} rapidly decreased due to quick discharge of the injected charges through the ultra-thin tunneling layer in the defect sites of a-Si layer. The memory window of this device is 6.71% retained after 10 years. Therefore, the suppression of this result due to the ultra-thin tunnel layer is insufficient to block the charge leakage from the a-Si to the Si substrate at room temperature. The ultra-thin tunnel oxide layer is not so good for device fabrication. Therefore, the ultra-thin tunnel oxide devices will result in poorer retention ability [19].

The retention characteristics of MOSOS devices were studied with thicker tunneling OSO stack layers of thicknesses 20/10/3.9 nm, respectively, and was observed an improvement of initially 6.03 V and decreased to 3.22 V after 10 years (shown in Fig. 4). This thicker tunneling layer gives a high P/E operation voltage of $\pm$ 12 V due to lowering the electric field on the tunneling layer [19]. As a conclusion, the 3.9 nm thicker tunnel layer is sufficient to block the charge leakage from the a-Si to the Si substrate at room temperature. The longer data retention OSO stack with the 3.9 nm thicker tunneling layer maintained about 53.39% after 10 years, whereas the 2.7 nm thin tunneling layer of OSO stack maintained about 6.71% after 10 years. The trapped charges loss can be reduced by increasing the thickness of the tunnel layer [20,21].

Finally, we investigate the charge retention characteristics of the MOSOSOS devices (shown in Fig. 5) with an OSOSO stack of thicknesses 20/5/2.7/5/2.7 nm, respectively. It was initially 3.85 V and decreased to 2.06 V after 10 years. It can be operated $\pm$ 10 V (P/E) bias keeping the time of 10 s fixed. The multilayer or stacked tunnel/trapped charge layers concept seems to be a promising solution due to the redistribution of the electric field across the tunnel stack compared to a single tunnel layer. In the single layer memory, electrons pass through one oxide tunneling barrier, while in the doubly stacked memory, the tunneling will be governed by the multiple energy barriers [13], resulting in less charge leakage of electrons from the a-Si.

Wang et al. [22] reported the charge storage in self-aligned double stacked Si nanocrystals in a SiN_x dielectric. This device structure is similar to ours. The doubly stacked a-Si can act as a good storage. As shown in Fig. 4(a), a great amount of charge loss takes place in the conventional device, which leads to obtaining only 6.71% of the extracted data retention in a single ultra-thin tunnel oxide device after 10 years. In comparison, as shown in Fig. 5, the extracted data retention of the 2.7 nm ultra-thin tunneling layer in the multi-stacked device remains ~54% of data retention. Therefore, the double stacked tunnel barrier exhibits excellent resistance to the charge retention loss. Improvements of the charge storage and retention can be undertaken due to the second tunneling barrier and second trap layer. Table 1 summarizes the electrical properties of all (MIS type) capacitors for comparison. These results indicate that thicker tunneling and multi-stacked devices can provide improved retention characteristics due to the efficient tunneling function of the modified layer thickness and structure than the thin tunneling layer devices.

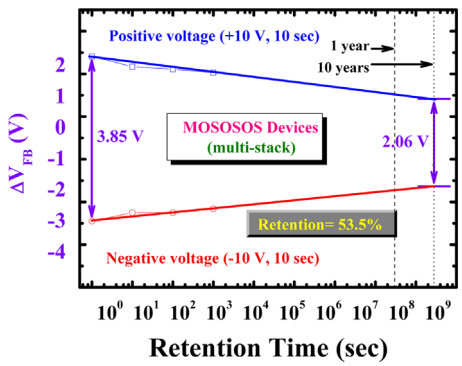

Fig. 5. Charge retention characteristics of fabricated MOSOSOS devices with OSOSO stack 20/5/2.7/5/2.7 nm thick.

4. Conclusion

The fabrication of the MOSOS and MOSOSOS devices with an OSO structure with thicker tunneling layer (3.9 nm) and an OSOSO, a multi-stacked structure with thin tunneling (2.7 nm) are presented. These devices exhibit improved retention characteristics with memory window loss after 10 years is ~46%. However, this is ~94% for thin tunneling OSO devices with 2.7 nm tunneling layer. Conversely, approximately 2–3 times larger memory windows were obtained from thicker tunneling layer of OSO stack or OSOSO multi-stack based devices. These devices using an a-Si, as charge-trap layer, could be applied to fabricate a NVM device for the memory integration of SOP displays.

Table 1
Charge storage and retention characteristics of different MIS type capacitors.

Devices	MOSOS (20/10/2.7 nm)	MOSOS (20/10/3.9 nm)	MOSOSOS (20/5/2.7/5/2.7 nm)
ΔV_{FB}	6.54 V at $\pm$ 10 V	12.64 V at $\pm$ 15 V	14.39 V at $\pm$ 15 V
Data retention after 10 years	6.71%	53.39%	~53.50%

Acknowledgments

This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2010-0020210) and by the Human Resources Development Program (No. 20124010203280) of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) grant funded by the Korea Government Ministry of Trade, Industry and Energy.

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