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Boosting the mobility and bias stability of oxide-based thin-film transistors with ultra-thin nanocrystalline InSnO:Zr layer

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Extensive attention on high-definition flat panel displays is the driving force to fabricate high-performance thin-film transistors (TFTs). A hybrid oxide TFTs fabricated using an interfacial layer of nanocrystalline Zr-doped InSnO (*nc*-ITO:Zr) and an amorphous InSnZnO films as an active channel is reported here. Due to the presence of *nc*-ITO:Zr layer, an improvement of the field-effect mobility (86.4 $cm^2/V{\cdot}s$) and threshold voltage (0.43 V) values for TFTs are observed. Positive gate bias stress study indicates the role of *nc*-ITO:Zr layer in fabricated TFTs through the suppression of charge trapping capability between the channel and insulating layer. © *2015 AIP Publishing LLC*.
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Amorphous silicon (a-Si) based thin-film transistors (TFTs), used in pixel-driving circuits to convert digital information into a visible image, have reached their performance limit in terms of enhancement of the display resolution and refresh rates. Nowadays, amorphous multi-component oxide-semiconductors are one of the building blocks of such active matrix flat-panel displays.[1] In particular, the ZnO-based TFTs, including InGaZnO,[2,3] ZnSnO,[4] HfInZnO,[5] and InSnZnO (ITZO)[6,7] have drawn considerable attention, due to their excellent sub-threshold swing ($SS < 0.4$ V/dec), better field-effect mobility ($\mu_{FE} \sim 10$–$25\ cm^2/V{\cdot}s$), and higher on/off current ratio ($I_{on/off} > 10^7$), compared with a-Si based TFTs. For large-size, high frame rate (>240 Hz) 3D and/or super hi-vision (7680×4320) active-matrix organic light-emitting diode (AM-OLED) displays, the mobility requirement is generally predicted to be over $30\ cm^2/V{\cdot}s$,[2] including the superior gate bias stability during device operation. Achieving both improvements simultaneously for ZnO-based devices are still challenge, because of gate bias-induced instabilities,[3,8] which could be realized as a change in threshold voltage (V_T), and/or μ_{FE}, and SS. Huh *et al*. observed that the Ga-rich InGaZnO TFT lead to a better gate bias stability, but had a lower μ_{FE}.[3] The highest μ_{FE} of $160\ cm^2/V{\cdot}s$ has reported in the Al/Ca-capped a-IGZO TFTs.[9] However, these oxide TFTs with a Ca diffusion normally suffer from an unacceptably large V_T (−25 V) and unstable electrical performances.

To address these issues, we introduced an ITO:Zr conducting oxide layers in our TFT devices. In this work, we have fabricated a high performance amorphous and crystalline phase metal-oxide hybrid TFTs, using combination of a-ITZO/*nc*-ITO:Zr thin films. The *nc*-ITO:Zr film can act as a mobility booster, and also improve the positive gate bias stability of the fabricated TFT devices. The ITO:Zr film is a highly degenerate n-type semiconductor, with a free carrier density (N_d) of $>10^{20}\ cm^{-3}$, and a preferential crystal orientation,[10] which lead to considerably efficient charge transport in the film. Moreover, it has been reported that ITO:Zr film has good chemical and thermal stability.[10] For a good quality of TFT devices, one can obtain the smallest SS (0.272 V/dec), highest μ_{FE} ($\sim 86.4\ cm^2/V{\cdot}s$), and lowest V_T (0.43 V) values, which can be achieved, through controlling the N_d and grain size (G_s) of the *nc*-ITO:Zr film by optimizing the deposition temperature. We demonstrate the influence of the *nc*-ITO:Zr interfacial layer on the electrical properties and gate bias stability of our hybrid TFT devices.

The bottom-gate structure a-ITZO/*nc*-ITO:Zr TFT devices (illustrated in the inset of Fig. 1) were fabricated on a

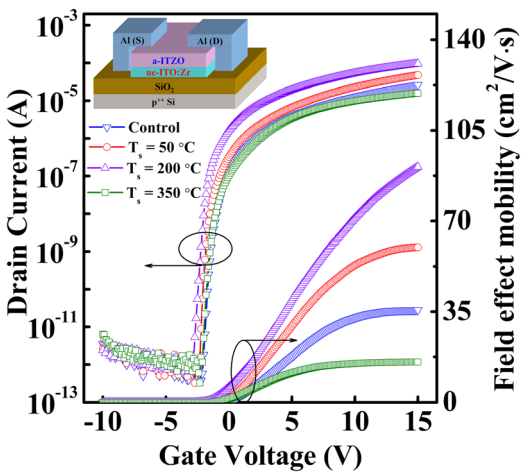

FIG. 1. Transfer characteristics of a-ITZO/ITO:Zr TFT devices with different T_s of ITO:Zr interfacial layer. In inset, schematic structure of these hybrid devices is shown.

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TABLE I. Device parameters extracted from the transfer curves of a-ITZO/ITO:Zr TFTs with different T_s of ITO:Zr interfacial layer.

T_s	Control	50 °C	200 °C	350 °C
$I_{on/off}$	2.25×10^7	5.61×10^7	8.83×10^7	1.40×10^7
V_T (V)	1.05	0.84	0.43	1.37
SS (V/dec)	0.274	0.275	0.272	0.281
μ_{FE} (cm^2/V.s)	35.3	60.3	86.4	15.6

thermally grown SiO_2/p^{++} Si substrates. Heavily doped Si and 100-nm-thick SiO_2 were used as a gate electrode and insulator layer, respectively. The 4-nm-thick ITO:Zr thin film (as an interfacial layer) was deposited onto SiO_2/Si substrates using RF magnetron sputtering through a shadow mask for channel definition. The sputtering was carried out in Ar ambient with a working pressure of 1.5×10^{-3} Torr. During deposition, the substrate temperature (T_s) was varying from 50 to 350 °C. The RF power of the In_2O_3:SnO_2:ZrO_2 target (90:9.8:0.2 wt. %) was fixed at 120 W. Subsequently, a 26-nm-thick a-ITZO film was deposited on an ITO:Zr/SiO_2/Si substrate using a target of In_2O_3:SnO_2:ZnO (30:35:35 at. %) with a power of 80 W using DC magnetron sputtering at room temperature. The working pressure was maintained at 5×10^{-3} Torr using a gas mixture of $Ar/O_2 = 14/6$ (sccm/sccm) in the chamber. Finally, the samples were annealed in air for 1 h at 300 °C. A 30-nm-thick a-ITZO TFTs (device A or control device) without interfacial layer were also prepared for comparison. Finally, a 150-nm-thick Al source/drain (S/D) electrodes were thermally evaporated on top of the channel layer through a shadow mask. The channel width (W) and length (L) of our TFTs were 200 μm and 200 μm, respectively.

The structural, surface morphological, and elemental analyses were carried out using X-ray diffraction (XRD, Bruker D8 Discovery), atomic force microscopy (AFM, SPA-300HV), and X-ray photoelectron spectroscopy (XPS, ESCA 2000, VG Microtech), respectively. The electrical characteristics of fabricated TFT devices were done by ELECS EL420C semiconductor parameter analyzer in a dark box.

Figure 1 presents a comparison of the transfer characteristics for TFT devices with a-ITZO (device A/control), and with an interfacial layer of ITO:Zr in between the a-ITZO and SiO_2 layer for different T_s. The optimum hybrid TFT device, which was fabricated at T_s of 200 °C (device B), is shown as the best device performance (high μ_{FE} of 86.4 cm^2/V·s, low V_T of 0.43 V, and high $I_{on/off}$ ratio of 8.83×10^7) compared to others. The values of μ_{FE}, V_T, and $I_{on/off}$ for the control single-layer a-ITZO TFT are obtained 35.3 cm^2/V·s, 1.05 V, and 2.25×10^7, respectively, as shown in Table I. We observed that the drain-current (I_{ds}) exhibits a three-fold increment from 2.67 to 9.18 μA at fixed drain voltage ($V_{ds} = 3$ V), for the fabricated device B, as compared with the control device. This is beneficial for operating a high-speed pixel circuits for large-sized 3D AM-OLED displays. In addition, the interfacial ITO:Zr layer are not influencing any additional defects in hybrid TFTs, as we can confirm from less change in SS values. Table I summarizes the device parameters extracted from the transfer curves, as shown in Fig. 1.

The improvement of parameter values in TFT devices with interfacial ITO:Zr films are confirmed by electrical, structural, and surface morphological studies. In order to study the microstructure of the interfacial ITO:Zr thin films, the XRD (shown in Fig. 2(a)), characterization was performed. The crystal quality of the ITO:Zr film grown at 200 °C is highly crystalline, with (400) preferred orientation, mixed with a small amount of the (222) phase. This result is consistent with Zhang *et al.*[10] and Raoufi *et al.*[11] The (400) phase contributes to the oxygen deficiency (V_O) state in the film, which influencing the mobility. Furthermore, the average G_s of the films at $T_s = 50$, 200, and 350 °C was estimated by Scherrer's equation[12] along the full width half maxima of the (222) and (400) diffraction peaks, which are 28, 37, and 51 nm, respectively. Our results are consistent with previous report on InSnZrO.[13] XRD investigations revealed that the ITO:Zr film structure (phase transitions: amorphous → nanocrystalline → polycrystalline) varies with increasing of T_s. Generally, low temperature deposited film has the probability

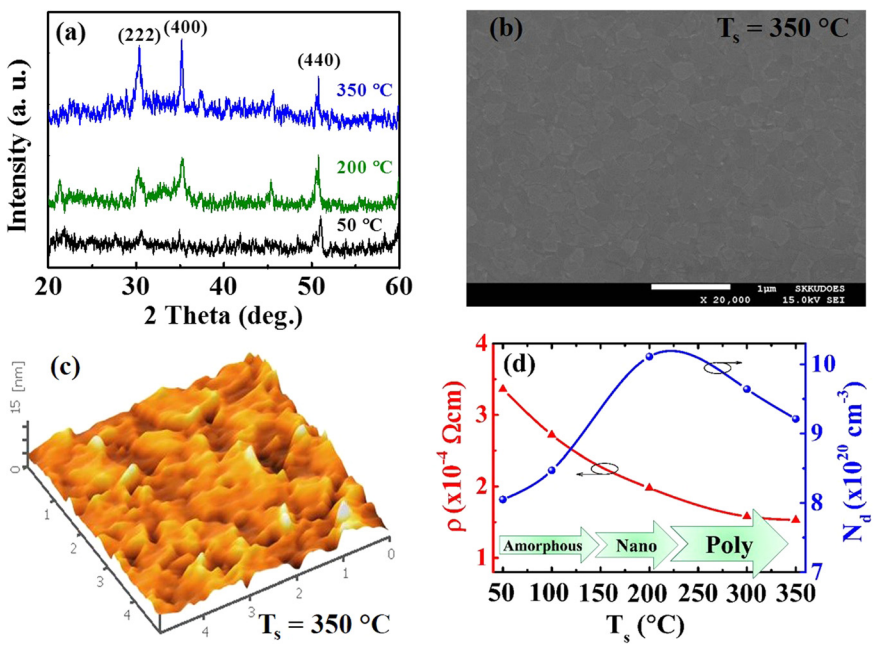

FIG. 2. (a) XRD patterns of ITO:Zr thin films at various T_s. (b) SEM and (c) AFM of ITO:Zr film deposited T_s at 350 °C. (d) Variations of ρ and N_d of ITO:Zr films as a function of T_s.

to form amorphous phase with small nucleus grains. The free electron moves faster in well-ordered crystalline phase rather than amorphous phase.[14] In contrast, at higher T_s (350 °C), the matrix vibration of the multi-component oxide films is accelerated, leading to polycrystalline (*pc*) structure with large columnar grains,[10,14] which is also confirmed (depicted in Fig. 2(b)) in scanning electron microscopic image (SEM, Hitachi S-4800).

The influence of T_s on the surface roughness of ITO:Zr film ($5\,\mu m \times 5\,\mu m$) was investigated by AFM. The surface roughness plays an important role in the electrical performance of the TFT devices,[8,15] and it has been found that the interfacial layers with a rough surface lead to worst overall device performance. The calculated root-mean square roughness (R_{rms}) increases with T_s, and was found to be 0.38, 0.54, and 1.52 nm for T_s of 50, 200, and 350 °C, respectively, which is consistent with the XRD (Fig. 2(a)) and XPS (Fig. 3(a)) results. The G_s and R_{rms} of ITO:Zr films are varying with T_s, which gives an evidence of improvement in film crystallization. However, at higher T_s (350 °C) causes the surface of film to become rougher ($R_{rms} = 1.52$ nm) with larger grains (51 nm), which is not suitable for TFT application. As a result, at T_s of 350 °C (device C) the inferior device performances (low μ_{FE} of $\sim 16\,cm^2/V{\cdot}s$, high V_T of 1.34 V, and low $I_{on/off}$ of 1.40×10^7), which may be due to the presence of scattering centers[8,15] and charge trap sites in between a-ITZO and SiO_2. Bae *et al.* reported a highest surface roughness of ZnO channel yields, the worst TFT device characteristics.[15] Similarly, Fujii *et al.* have also reported that high pressure (1.0 MPa) annealed IGZO film shows higher film roughness, which deteriorates the TFT performances.[16]

Further, the variation of resistivity (ρ) and N_d of ITO:Zr films grown on glass as a function of T_s was studied using Hall measurement (Ecopia HMS-3000). Fig. 2(d) shows that the N_d is varied from 8.05×10^{20} to $1.01 \times 10^{21}\,cm^{-3}$ with the change of T_s from 50 to 200 °C. The ρ of the film is found to decrease with increasing T_s and reach about $1.53 \times 10^{-4}\,\Omega$ cm at 350 °C. This increase in electrical conductivity is due to the increase in N_d. The N_d increases with T_s may be due to the diffusion of Sn and Zr atoms into In-cation sites in the In_2O_3 matrix[17] and the generation of V_O. However, at higher T_s (350 °C), the N_d of film were slightly decreasing ($9.21 \times 10^{20}\,cm^{-3}$) related with reducing V_O. The population of V_O substitution of Sn and Zr atoms into the In_2O_3 matrix are confirmed from XPS spectra of the O1s peak in ITO:Zr films (in Fig. 3(b)). Gaussian fitting was used for the de-convolution of the O1s peaks at 530.2 ± 0.1 eV (O_I), 531.7 ± 0.1 eV (O_{II}), and 533.1 ± 0.2 eV (O_{III}), respectively.[18] The V_O of the films at different $T_s = 50$, 100, 200, 300, and 350 °C were estimated by the ratio of peak area ($O_{II}/O_I + O_{II}$), which are 21.11%, 21.89%, 23.17%, 23.91%, and 23.24%, respectively. It is to be noted that the increase in V_O can be implied by the enhancement of the (400) peak. The core level of the O1s region and In/Sn ratio for various T_s (50, 200, and 350 °C) are plotted in Figs. 3(a) and 3(b), respectively. It is observed that the In/Sn ratio is increased with increasing T_s. In addition, the lowering binding energy of the O1s peak of higher T_s (>300 °C) films suggests that the microstructural changes (to form polycrystalline) due to

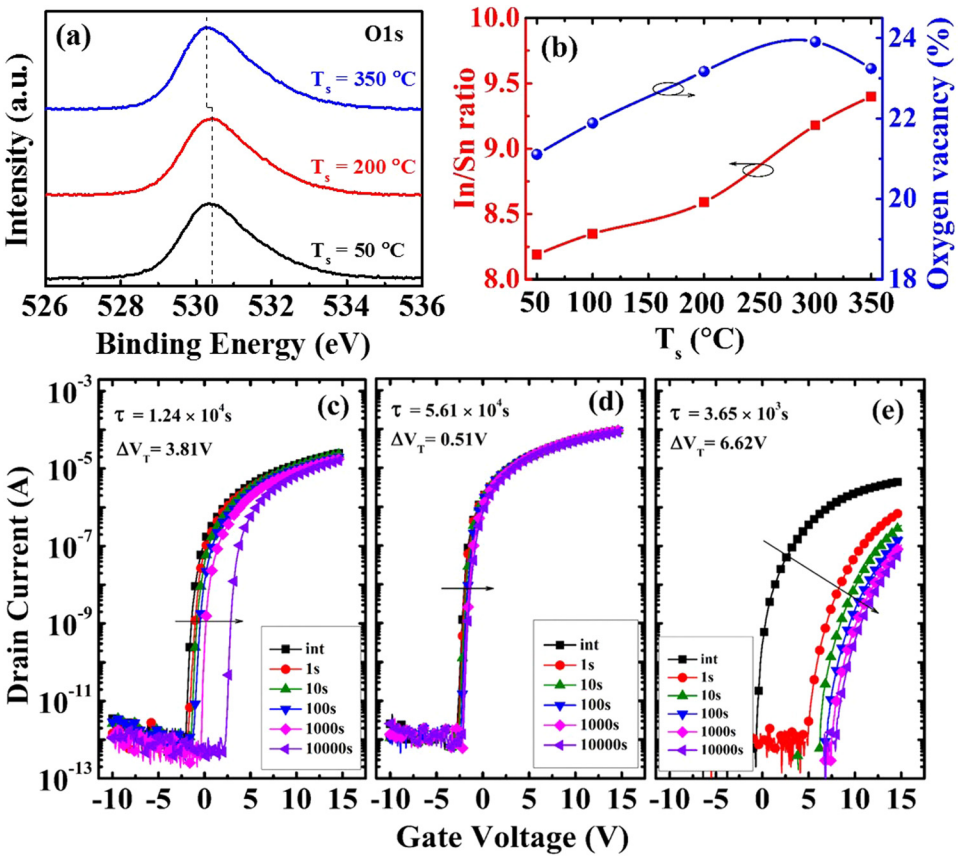

FIG. 3. (a) XPS spectra of O1s region of ITO:Zr thin films various T_s. (b) Variation of In/Sn ratio and V_O as a function of T_s. The evolution of the transfer curves for (c) device A, (d) device B, and (e) device C as a function of the positive applied stress time.

the random distribution of particles (see Fig. 2(c)), which is an evidence for the decreases in the N_d and V_O.

Furthermore, we noted that the interfacial film not only acts as an electron enhancement layer but also as a capping layer to improve the positive gate bias stress (PGBS) stability. A gate bias stress of +15 V at $V_{ds} = 3$ V was applied to the fabricated TFT devices for a period of 10^4 s to evaluate the device stability. Figs. 3(c), 3(d), and 3(e) show the evolution of the transfer characteristics for device A, device B, and device C TFTs, respectively. A typical positive V_T shift (ΔV_T) of transfer curves are observed, which may be due to field-induced electron-trapping[8] and without a change in the SS. Compared to device A ($\Delta V_T = 3.81$ V, with little change in μ_{FE}), the better stability of the TFT device is achieved in device B ($\Delta V_T = 0.51$ V, with no change in μ_{FE}), which may be attributed to minimize the charge trapping due to the introduction of *nc*-ITO:Zr interfacial layer. The electron trapping is dominant in device A, due to the excess oxygen in active layer. The electrical stability of oxide based TFTs with excess oxygen[19,20] in their active layers degrades due to the defects in the channel/gate insulator interface and/or acceptor-like defects in the bulk of channel layer. However, the stability of device C is worse ($\Delta V_T = 6.62$ V, with huge change in μ_{FE}) due to the induced charge trapping by insertion of *pc*-ITO:Zr layer. The measured ΔV_T values are well matched with the stretched-exponential model,[21] which originates from the charge being trapped at the channel/insulator interface or getting injected into the insulator (excluded insulator influences, as the high quality SiO_2 is used to fabricate the TFTs). The obtained charge trapping times (τ) are 1.24×10^4 s, 5.61×10^4 s, and 3.65×10^3 s for device A, device B, and device C, respectively, which are consistent with a previous report by Lopes *et al.*[21] A higher τ value suggests that the trapping of fewer electrons during the gate bias stress which leads to a more stable device performance. The excess of oxygen in a-ITZO channel layer induced charge trapping during the PGBS, which may be resisted, due to insertion of the (oxygen free) *nc*-ITO:Zr layer. The Zr ions act as strong oxygen binders (higher bonding energy = 776.1 kJ mol^{-1}) compared to Zn in the ITO:Zr layer,[22] which might be the reason to improve stability in the hybrid TFT devices.

In summary, a comparison on electrical performance of a-ITZO TFTs with and without *nc*-ITO:Zr interfacial layer is discussed here. Optimization of the substrate temperature during processing for the *nc*-ITO:Zr layer to fabricate the TFTs is shown based on structural and electrical studies. With an ITO:Zr thin film G_s of ~37 nm and N_d of 1.01×10^{21} cm^{-3}, the best device performance ($\mu_{FE} = 86.4$ $cm^2/V{\cdot}s$ and $V_T = 0.43$ V) is achieved, compared to those ($\mu_{FE} = 35.3$ $cm^2/V{\cdot}s$ and $V_T = 1.05$ V) of the control TFT. Such a-ITZO/*nc*-ITO:Zr hybrid TFT devices may be a promising approach for making super hi-vision display panels.

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